CLAIMS

What is claimed is:

1. A method for avoiding a step height over a readable laser marked portion of a process wafer comprising the steps of:

providing a process wafer comprising active area trenches and at least one inactive area trench formed overlying at least a portion of a laser marked portion;

forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches;

forming a resist layer comprising patterned portions disposed between the active area trenches and the at least one inactive area trench;

removing the filling layer portions not covered by the resist layer;

removing the resist layer; and,

planarizing the wafer process surface wherein the active area trenches and the at least one inactive area trench are substantially co-planar.

2. The method of claim 1, wherein the planarization process comprises a chemical mechanical polish (CMP) process.

3. The method of claim 1, wherein the step of removing the filling layer portions comprises a dry etching process;

4. The method of claim 1, wherein the laser marked portion comprises an exclusion area at the process wafer periphery adjacent the process wafer peripheral edge.

5. The method of claim 1, wherein the active area trenches comprise shallow trench isolation (STI) trenches.

6. The method of claim 1 wherein the process wafer comprises a silicon substrate and at least one overlying nitride layer.

7. The method of claim 1, wherein the filling layer is selected from the group consisting of silicon dioxide and silicon oxynitride.

8. The method of claim 1, wherein the patterned portions comprise a linear shape extending adjacent the length of the active area trenches.

9. The method of claim 1, wherein the patterned portions comprise a width of greater than about 1.5 mm.

10. The method of claim 9, wherein the patterned portions comprise at least two lines having a linewidth of from about 10 microns to about 500 microns with a pitch from about 1 to about 4 times the linewidth.

11. A method for eliminating a step height over a readable laser marked portion of a process wafer to improve a subsequent patterning process over adjacent active areas comprising the steps of:

providing a process wafer comprising an active area including shallow trench isolation (STI) trenches and at least one trench formed in an adjacently disposed inactive area overlying a laser marked portion of the process wafer comprising readable information;

blanket depositing a layer of filling material over the process wafer surface;

forming a resist layer comprising first patterned portions overlying the active area and an unpatterned portion overlying the inactive area;

lithographically patterning the resist layer to form second patterned portions disposed between the active area and the inactive;

carrying out an etching process to etch through a thickness of exposed portions of the filling material according to the first and second patterned portions;

removing the resist layer; and

carrying out a CMP process to planarize the wafer process surface including the active area and the inactive area without an intervening step height.

12. The method of claim 11, wherein the laser marked portion comprises an exclusion area at the process wafer periphery.

13. The method of claim 11, wherein the process wafer comprises a silicon substrate and at least one overlying nitride layer.

14. The method of claim 11, wherein the filling material is selected from the group consisting of silicon oxide and silicon oxynitride.

15. The method of claim 11, wherein the first patterned portions comprise a reverse tone pattern.

16. The method of claim 11, wherein the second patterned portions comprise lines extending adjacent the length of the active area.

17. The method of claim 11, wherein the second patterned portions comprise a width of greater than about 1.5 mm.

18. The method of claim 11, wherein the second patterned portions comprise at least two lines having a linewidth of from about 10 microns to about 500 microns with a pitch from about 1 to about 4 times the linewidth.

19. The method of claim 11, wherein the step of lithographically patterning comprises inserting a second mask comprising an image of the second patterned portions between the process wafer surface and a first mask comprising an image of the first patterned portions.

20. The method of claim 11, wherein the readable information is selected from the group consisting of alphanumeric characters, numbers, and bar codes.

21. A semiconductor process wafer comprising:

active areas comprising active area trenches and at least one adjacent inactive area trench at least partially overlying a laser marked region; and

wherein said active area trenches and the at least one inactive area trench are backfilled with a filling layer to be substantially co-planar.

22. The semiconductor process wafer of claim 21, wherein the laser marked region comprises an exclusion area adjacent the semiconductor process wafer peripheral edge.

24. The semiconductor process wafer of claim 21, wherein the active area trenches comprise shallow trench isolation (STI) trenches.

25. The semiconductor process wafer of claim 21, wherein the semiconductor process wafer comprises a silicon substrate and at least one overlying nitride layer.

26. The semiconductor process wafer of claim 21, wherein the filling layer is selected from the group consisting of silicon dioxide and silicon oxynitride.

27. The semiconductor process wafer of claim 21, wherein the laser marked region comprises readable information selected from the group consisting of alphanumeric characters, numbers, and bar codes.

28. A semiconductor process wafer comprising:

active areas comprising shallow trench isolation (STI) trenches and an adjacent inactive area trench at least partially overlying a laser marked region; and

wherein said STI trenches and the inactive area trench are backfilled with a filling layer to be substantially co-planar.

29. The semiconductor process wafer of claim 28, wherein the laser marked region comprises an exclusion area adjacent the semiconductor process wafer peripheral edge.

30. The semiconductor process wafer of claim 28, wherein the semiconductor process wafer comprises a silicon substrate and at least one overlying nitride layer.

31. The semiconductor process wafer of claim 28, wherein the filling layer is selected from the group consisting of silicon dioxide and silicon oxynitride.

32. The semiconductor process wafer of claim 28, wherein the laser marked region comprises readable information selected from the group consisting of alphanumeric characters, numbers, and bar codes.